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Envelope Tracking RF Power Amplifiers: Fundamentals, Design Challenges, and Unique opportunities offered by LEES-SMART InGaAs-on-CMOS process

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Abstract

The RF power amplifier (PA) is often the most power dissipative block in a smartphone and it usually dissipates ~50% of the total power. One major drawback of the envelop tracking (ET) PA is the limited (and insufficient) bandwidth of its supply modulator. The emerging LEES-SMART InGaAs-on-CMOS process offers a higher operation speed (due to the high speed InGaAs transistors) and the capability for complex signal processing. In this paper, we present the fundamentals and design challenges of ET PA, and how the emerging LEES-SMART InGaAs-on-CMOS process may be exploited for a high power-efficiency.

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Keywords: envelop tracking; power amplifier; supply modulator; LEES-SMART; InGaAs-on-CMOS process

1. Introduction

The RF power amplifier (PA) [1] is often the most power dissipative block in a smartphone and it usually dissipates

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~50% of the total power. Hence, to extend the battery lifespan, it is imperative that the power-efficiency of the RF power amplifier is high. Of all reported methods to improve the power-efficiency of the RF PA, envelop tracking (ET) is probably the most promising – it features ~20% higher power-efficiency and this translates to ~10% longer battery lifespan.

At this juncture, one major drawback of the ET PA is the limited (and insufficient) bandwidth of its supply modulator (a key building block in the ET PA) [2, 3], hence the ensuing reduced data rate and/or reduced power-efficiency (but higher than that of a conventional linear PA). This is primarily due to the large parasitic capacitance of the output transistors of the supply modulator; for instance, for a typical output impedance of 0.2ohm, the parasitic capacitance can be a high >30pF.

The emerging InGaAs-on-CMOS process is currently being developed by LEES-SMART. This process integrates InGaAs transistors and silicon transistors on a single silicon wafer and it is advantageous over conventional silicon processes and the InGaAs -only processes. Compared to the former, it offers a higher operation speed (due to the high speed InGaAs transistors). Compared to the latter, it offers the capability for complex signal processing. We envision that by employing this process, unprecedented supply modulator bandwidth and unprecedented overall power-efficiency of the RF PA can be achieved.

In this paper, we will present the fundamentals and design challenges of ET PA, and how the emerging LEES-SMART InGaAs-on-CMOS process may be exploited for a high power-efficiency.

2. Review of envelop tracking power amplifier design

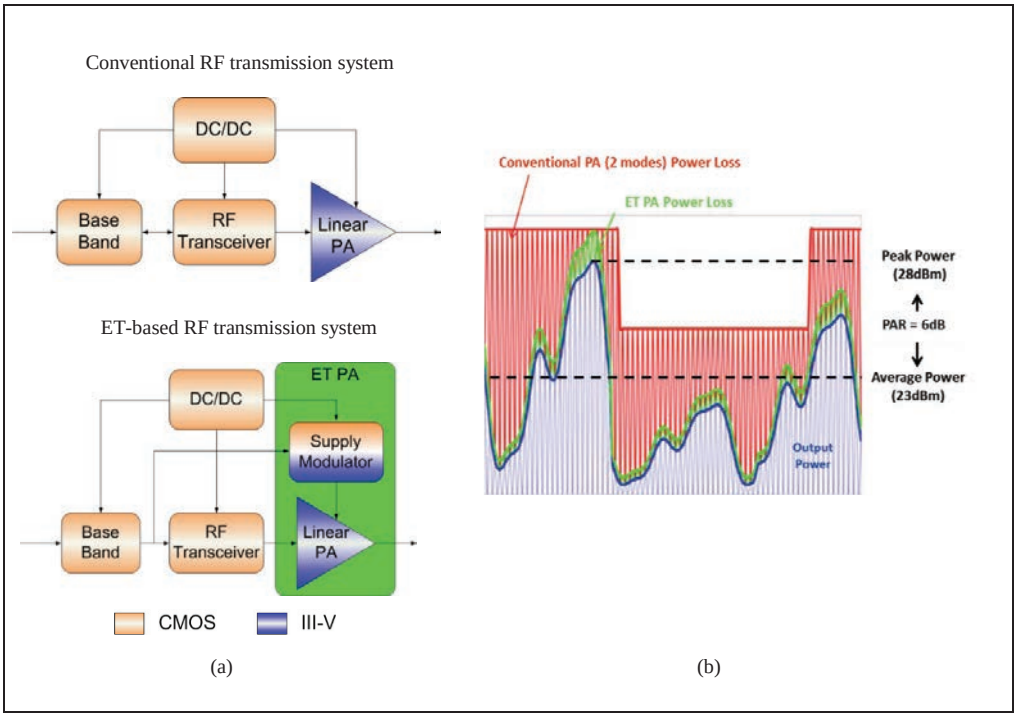

Fig.1. (a) Block diagram of conventional RF transmission system and ET-based RF transmission system (b) Power efficiency of conventional PA (2 modes) and ET PA

The block diagram of conventional RF transmission system and ET-based RF transmission system are depicted in Fig.1. (a). ET is proposed to boost the PA efficiency for high peak-to average ratios (PAR) signals, such as 4G LTE and WLAN. This ET-based architecture can be more effective than the conventional one as the PA supply voltage is constantly modulated by the supply modulator based on the output power. The comparison of the power-efficiency

of the ET PA against a conventional linear PA (2 modes) is depicted in Fig.1. (b). From the comparison, we can see that the power efficiency of ET PA has significantly improved compared to the conventional counterparts, especially when the output power is low.

The main design challenge of the ET-based transmission system is to design a wideband supply modulator delivering high output power to the linear PA. For instance, the 10MHz 4G LTE signals requires the supply modulator to deliver maximum output power ~5W @ 3.7V supply voltage and the bandwidth >10MHz. As mentioned in the earlier section, due to the large parasitic capacitance of the output transistors of the supply modulator, the bandwidth of the supply modulator are limited. In addition, designing high-linearity RF linear PA and handling noise arising from integration can also be challenge for designing high-fidelity and high-efficiency ET PA.

3. Proposed ET PA based on LEES-SMART InGaAs-on-CMOS process

The emerging LEES-SMART InGaAs-on-CMOS process provides a solution to integrate InGaAs transistors and CMOS transistors on a single silicon wafer. InGaAs transistors have lower parasitic capacitance, lower output impedance, higher operation speed and high power efficiency compared to conventional CMOS transistors. By taking the advantages of the LEES-SMART InGaAs-on-CMOS process, an integrated ET PA is proposed which embody CMOS signal processing circuits and InGaAs power transistors, shown in Fig. 2. In this architecture, InGaAs devices are employed in the Class D output stage and RF linear PA for higher output power and higher power efficiency and the Class D modulator is realized by the conventional CMOS devices.

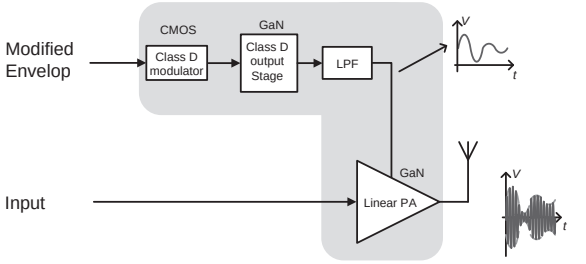

Fig.2. Block diagram of proposed ET PA based on InGaAs-on-CMOS process

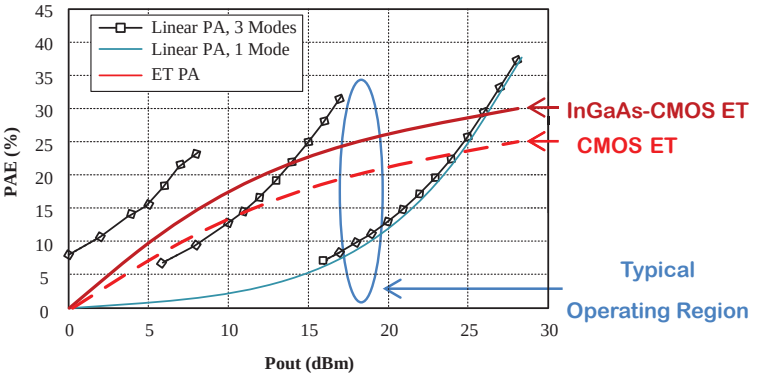

Fig.3. Comparison of the power efficiency of the ET PA and linear PA

The comparison of the power efficiency of the ET PA and the linear PA based on simulation results are depicted in Fig.3. The InGaAs-on-CMOS ET are expected to improve the power efficiency by ~ 5% at the typical operating region compared to the CMOS ET and it shows larger improvement compared to the normal linear PA (1 mode and 3 modes). It is worthwhile to notice that the speed of InGaAs devices is faster than the CMOS devices. It may push the bandwidth of ET PA using InGaAs-on-CMOS process beyond 20MHz, which is hardly realized by standard

CMOS process.

4. Conclusion

In this paper, we present that the major challenge of designing ET PA is the limited bandwidth. It is well known that InGaAs transistors have lower parasitic capacitance, lower output impedance, higher operation speed and high power efficiency compared its CMOS counterparts. By taking the advantages of the emerging LEES-SMART InGaAs-on-CMOS process, a novel ET PA based on InGaAs-on-CMOS process is proposed. In this architecture, InGaAs devices are employed in the Class D output stage and the RF linear PA design for higher output power and higher power efficiency and the Class D modulator are realized by the conventional CMOS devices. It is expected to have ~5% improvement on the power efficiency of the ET PA and higher bandwidth (bandwidth beyond 20MHz are expected) compared to the CMOS ET PA.

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